

FIG. 1

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FIG. 2

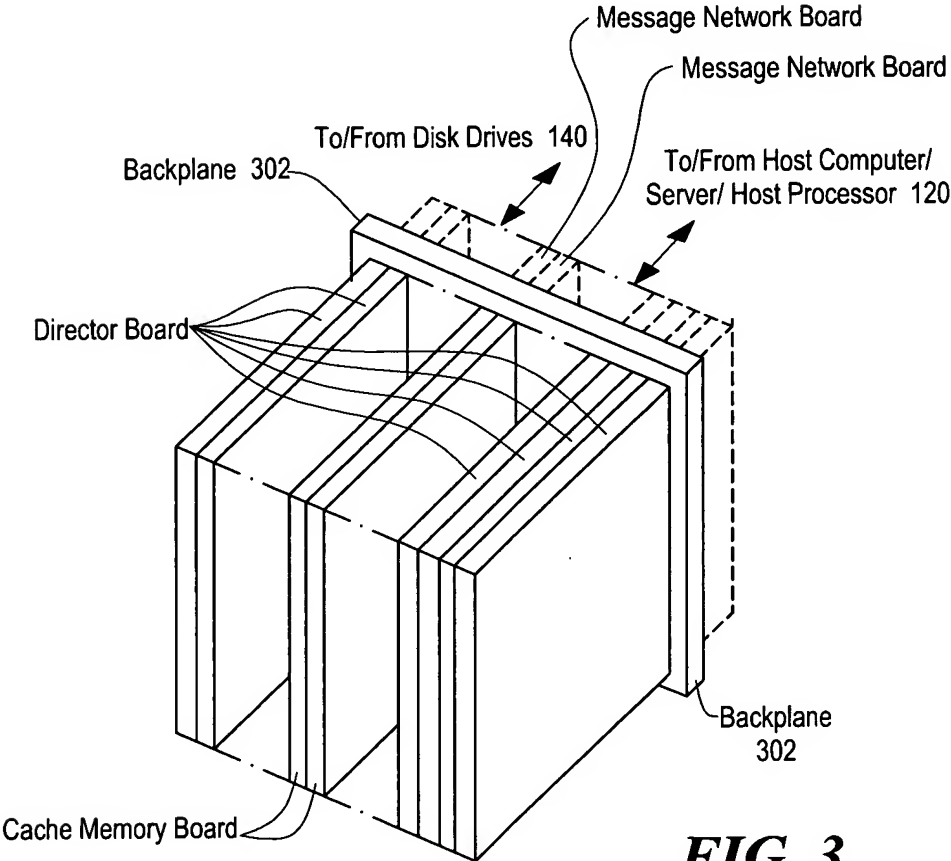
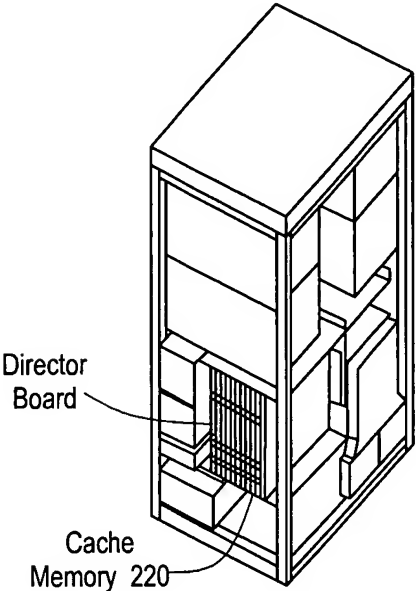


FIG. 3

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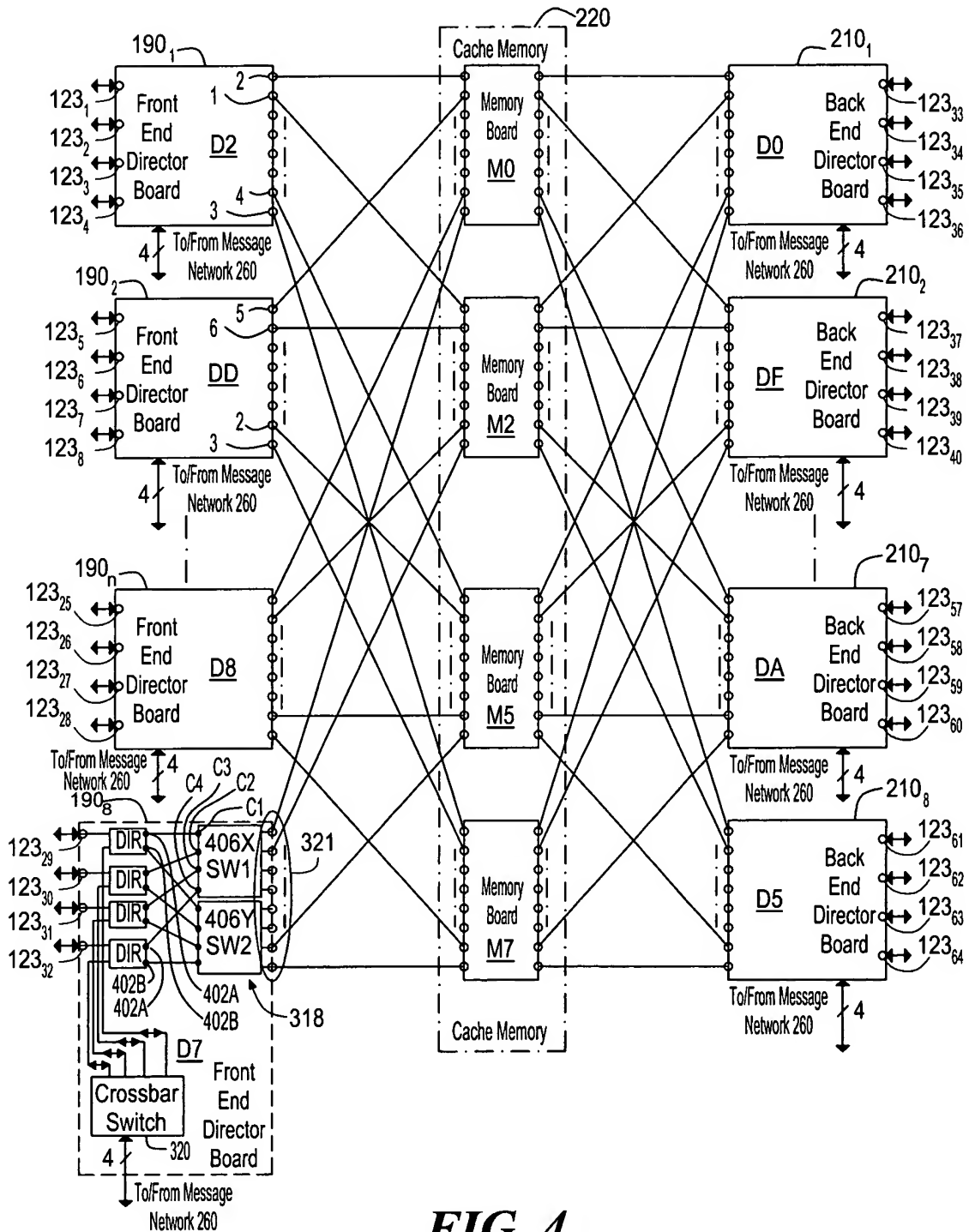


FIG. 4

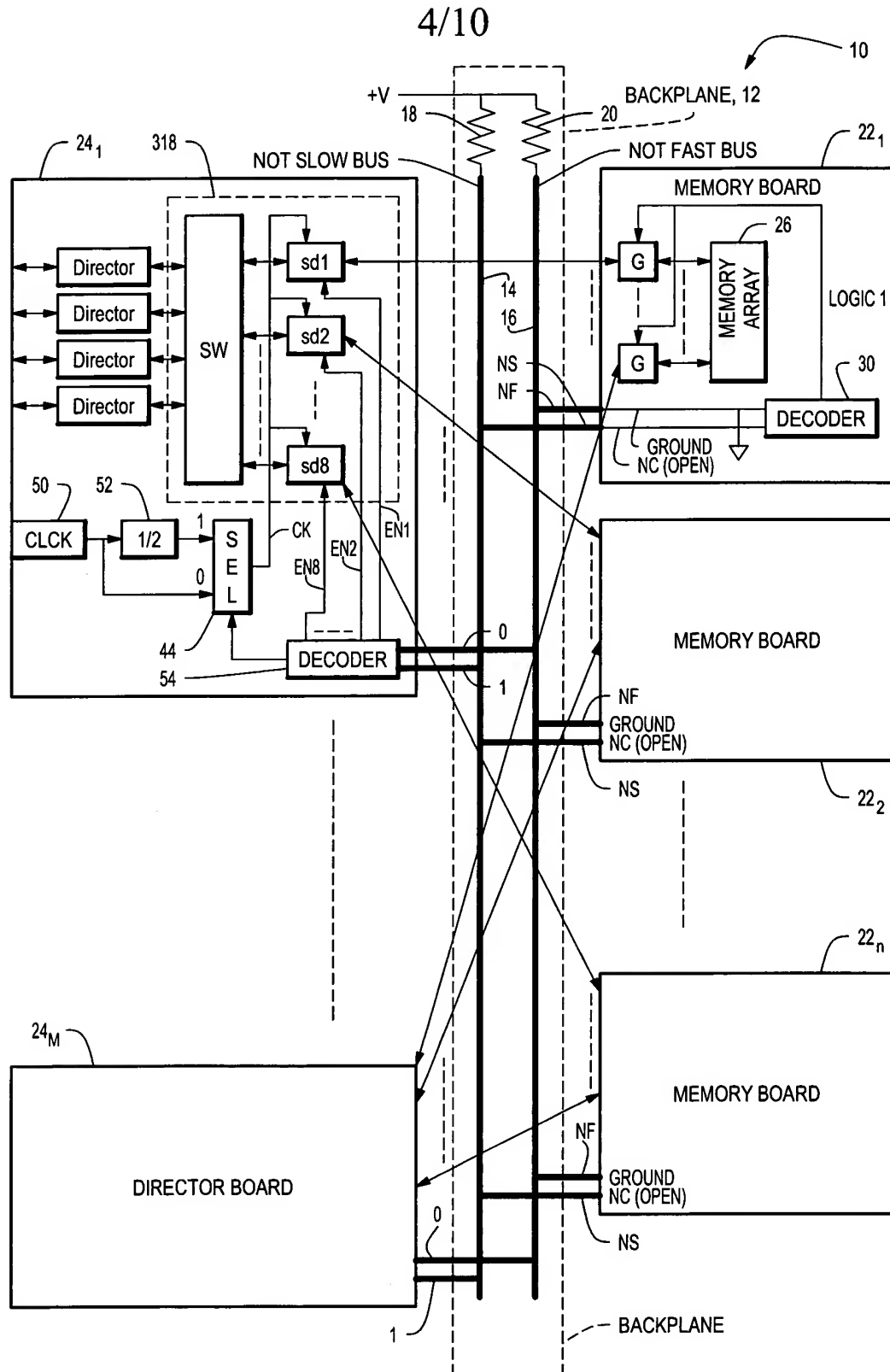


FIG. 5

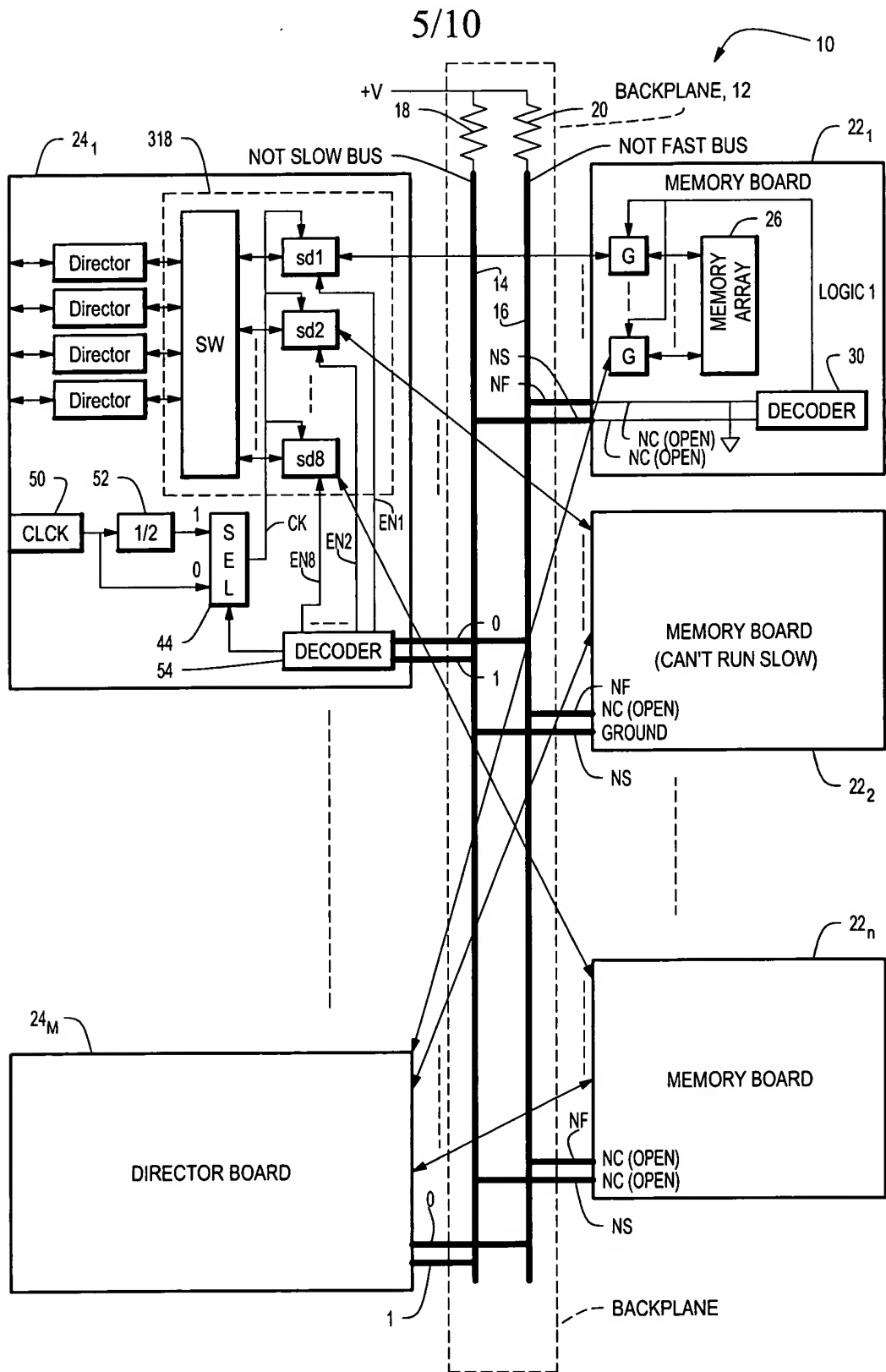


FIG. 6

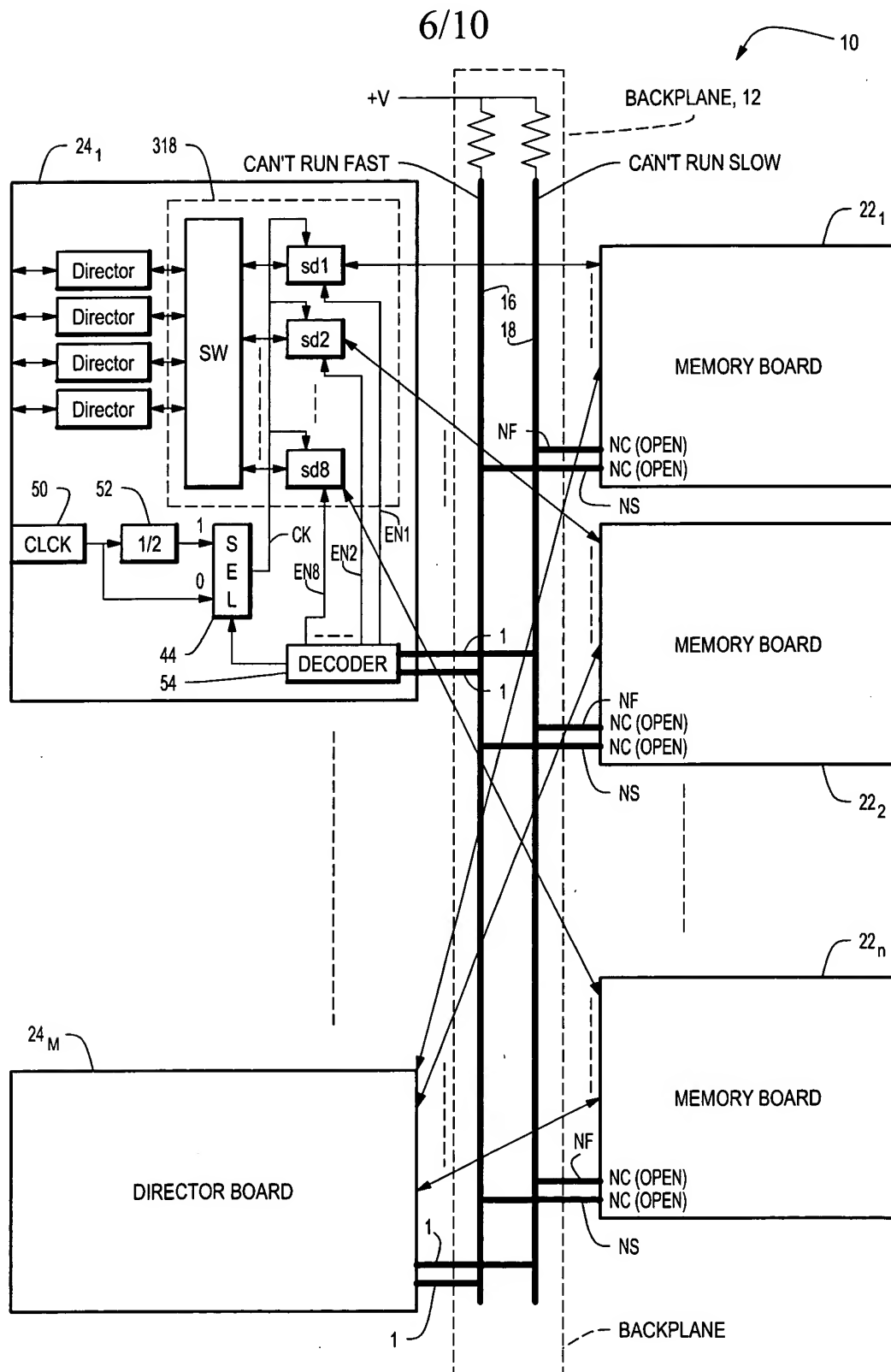


FIG. 7

SYSTEM HAVING BACKPLANE PERFORMANCE CAPABILITY SELECTION LOGIC

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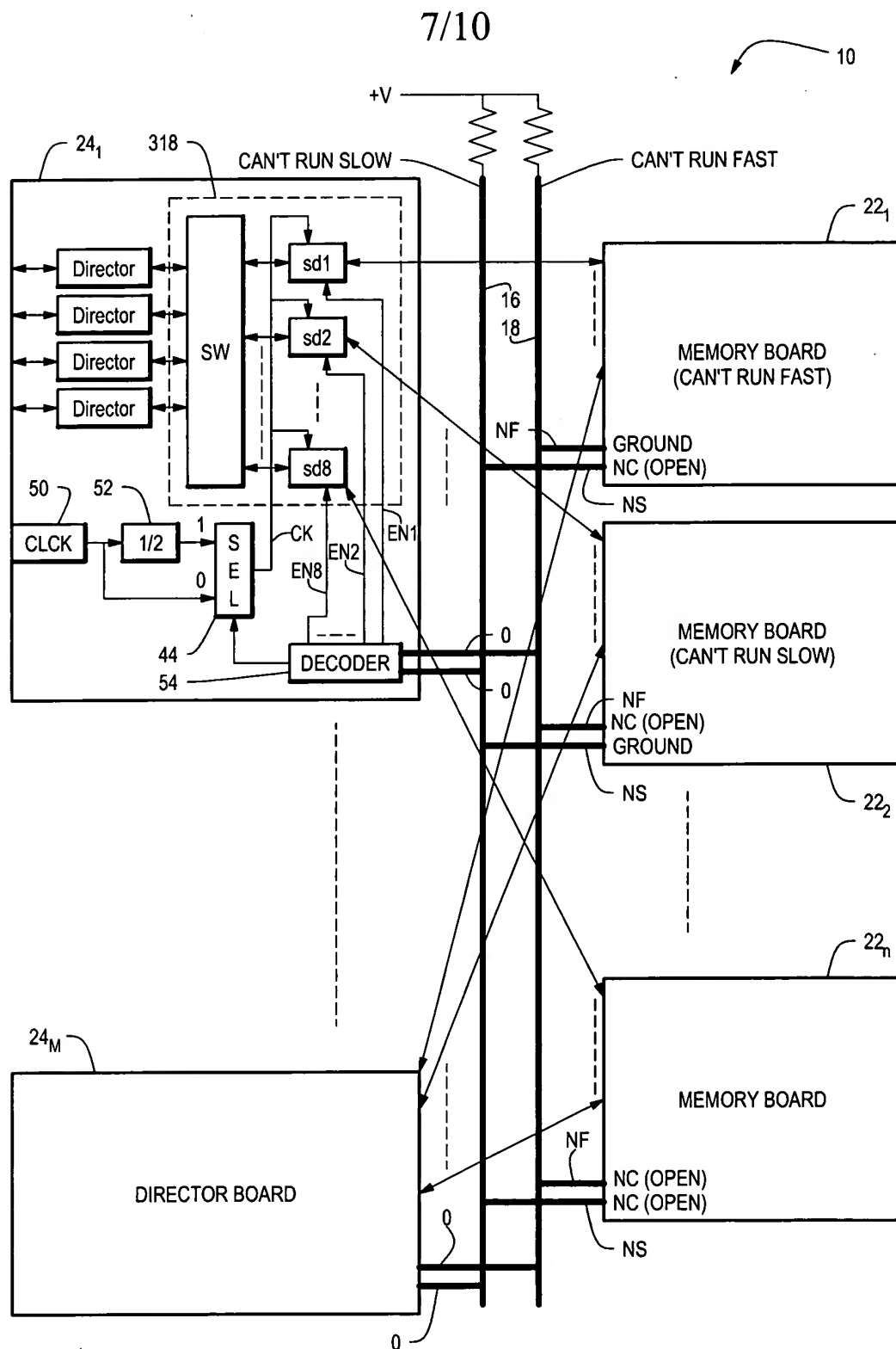


FIG. 8

SYSTEM HAVING BACKPLANE PERFORMANCE CAPABILITY SELECTION LOGIC

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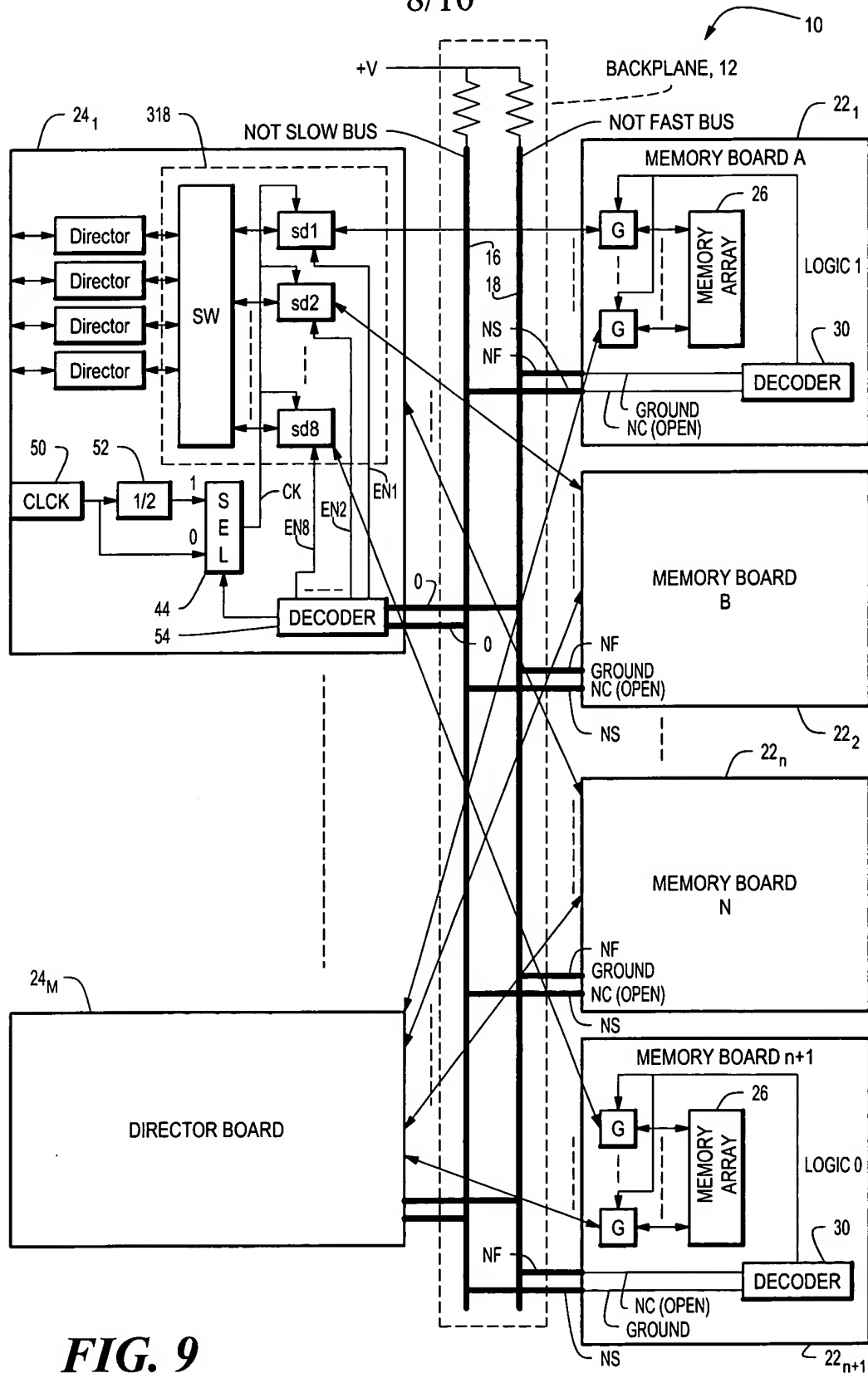


FIG. 9

SYSTEM HAVING BACKPLANE PERFORMANCE CAPABILITY SELECTION LOGIC

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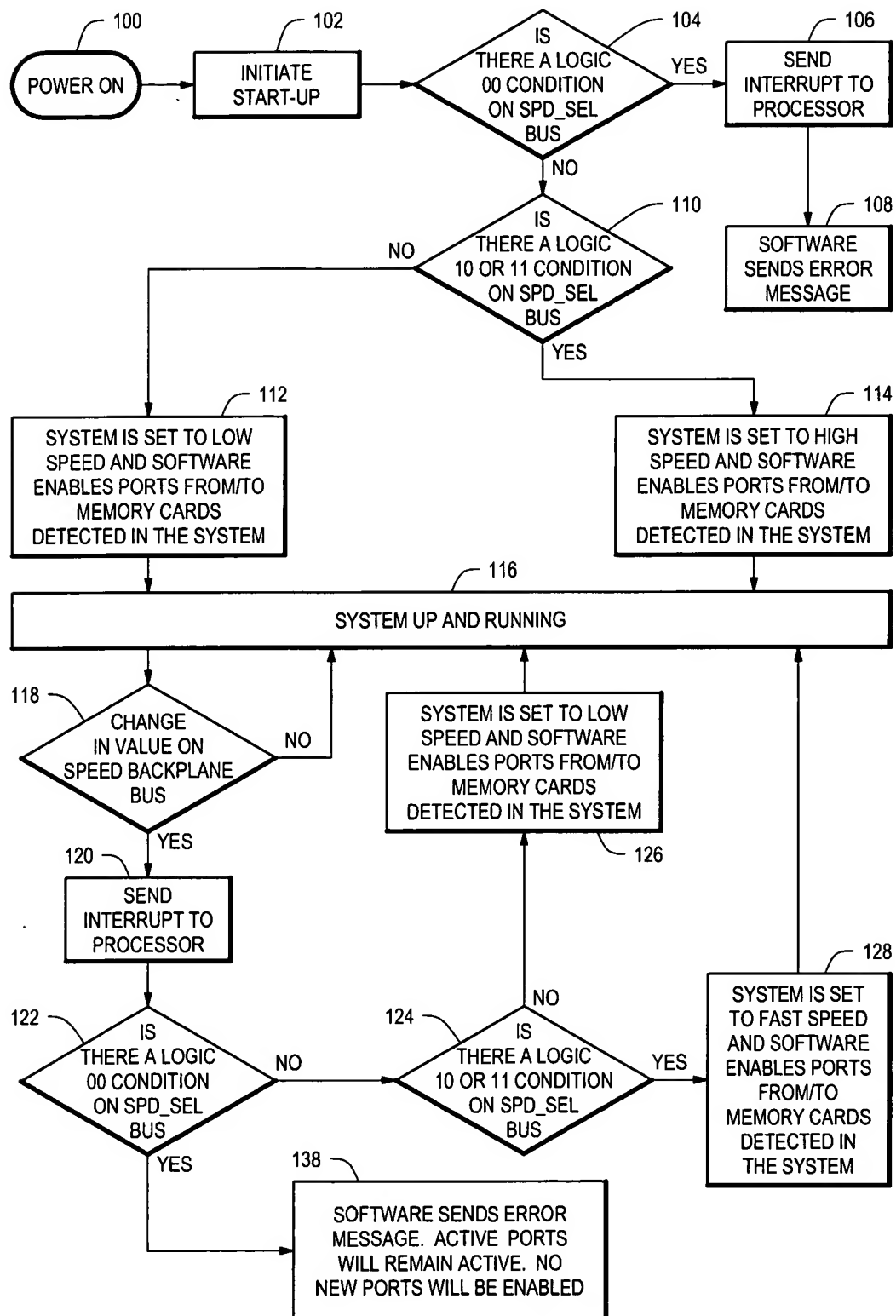


FIG. 10

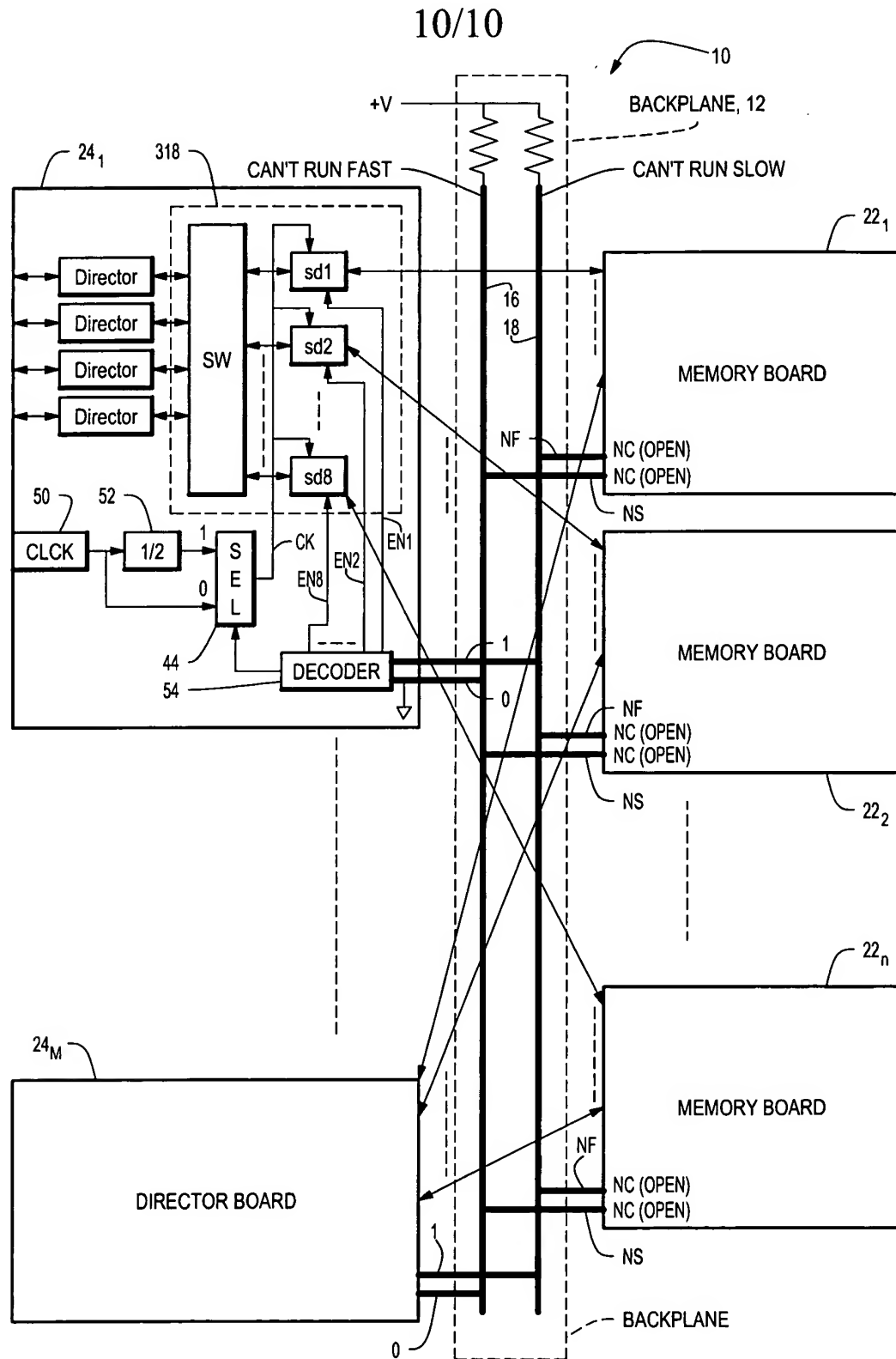


FIG. 11